Einfache und effiziente Inbetriebnahme und Test von Embedded Systemen

Pascal Willems (Presentation & Live Demo)
Embedded Computing Conference Winterthur
5. Juni 2018
FlowCAD – Your EDA-Partner
Moore’s Law was published on April 19, 1965 by Gordon E. Moore, who was working as the director of R&D at Fairchild Semiconductor.

The complexity of electronic circuits doubles approx. every 2 years: 
(Number of constraints)
Products / Solutions for Electronic Engineers

Solutions
- PCB Layout
- PSpice - Simulation
- SI- and PI-Simulation
- Multiphysics Simulation
- Thermal Simulation
- Timing Analyse
- 3D mCAD-eCAD Integration
- Reliability (MTBF, FTA, FMEA)
- CAM Verification
- Boundary Scan Test
- CAD-Flow Management
- PLM and ERP-Interfaces
Focus on Customer Satisfaction

Sales
• Fair, competent advice
• Long term solutions

Support
• Hotline, netviewer
• Survey

Service
• PCB Design Services
• (Layout, simulation, migration)

Training
• Training centers, on-site
• Workshops
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Why testing?
Test Technologies I

• Automated Optical Inspection (AOI)
  – Automated visual inspection of PCBs, using a camera to check for missing/misplaced components and quality defects with soldering or skewed components

• Automated X-ray Inspection (AXI)
  – The only other technology which can ‘see’ under BGA pins
  – Usually used in conjunction with a technology that actually checks physical operation of the board

Test Capabilities
  – Non-contact test
  – Can observe
    – solder quality
    – component skew problems

Limitations
  – Access to BGAs
  – Speed and access limits
  – No functional testing and programming
  – Ambiguous results
Test Technologies II

• Functional Circuit Test (FCT)
  – The oldest type of testing
  – Use the functionality of devices in the circuit to test the circuit as a whole

Test Capabilities
  – Tests devices at the full operating speed
  – Can be used in conjunction with test fixtures to get good test coverage

Limitations
  – Requires minimum functionality or tests will not run
  – Requires programming into board
  – May affect available space for board firmware
  – Failure diagnosis can be difficult
  – Long development time
Test Technologies III

• Bed-of-nails / In-Circuit Test (ICT)
  – State of the art, since the mid-1970s
  – Electrical probe test of a populated PCB

• Flying Probe (FPT)
  – Introduced in 1986, to provide an easy to use and dependable fixtureless tester for the manufacturing world

Test Capabilities
  – Checks for shorts, opens, resistance, capacitance to show whether the assembly was correctly fabricated

Limitations
  – Access to BGAs
  – Space on PCB for test points
  – High NRE / fixture costs (ICT)
  – Long test times (flying probe)
Test Technologies III

- Boundary Scan
JTAG / Boundary-Scan Testing – Benefits

• Designed to minimise access difficulties
  – 4 / 5 pin interface
  – Gives access to the whole device
  – JTAG devices connect to form a chain

• Abstracted from device and board complexity
  – No need to know what type of CPU core, or even whether the device is a CPU, FPGA, CPLD, RAM, PHY, etc.
  – Much reduced need for test points

• Test non-JTAG devices through the JTAG ones
  – Test or program most types of device by controlling the pins from a JTAG device
What is JTAG?

Each Boundary-Scan Cell can:

- Capture data on its parallel input PI
- Update data onto its parallel output PO
- Serially scan data from SO to its neighbour’s SI
- Behave transparently: PI passes to PO

**Note:** Boundary-scan cells represent virtual test points for the access to some nets.
JTAG / Boundary-Scan Testing – History

- **1985**: JETAG formed
- **1986**: JTAG replaces JETAG
- **1990**: JTAG / Boundary-Scan Testing – History
- **2003**: 1149.6 includes AC-coupled nets
- **2010**: 1149.7 includes two-wire JTAG
- **2013**: 1149.1-2013 revision
## Boundary-Scan Versus Other Test Methods

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What kind of error can be detected?
Extended Testing
Prototype bring-up

No Test Program needed
JTAG – getting it right

JTAG comes with some conditions

• You have to connect it - laws of physics still apply

• Signal integrity is important
  – For test time
  – For reliability
  – For programming speed

• There may be pins which need to be accessible
  – May need access to set the device into JTAG mode

• Design and layout of the JTAG signals makes a difference
  – Getting it wrong can double (or worse) the time taken to test each PCB
JTAG / Boundary-Scan IEEE 1149.1

Multiple devices connected to form a JTAG chain
Check Termination

Multiple devices connected to form a JTAG Chain
XJTAG DFT Assistant

- App (plug-in, add-on) to check the connection and termination of the Taps and show the test coverage for:
  - OrCAD
  - Allegro (CIS)
  - Mentor Pads
  - Mentor Expedition
  - Zuken CR8000
  - Altium
XJTAG DFT Assistant

• Getting the JTAG design right
  – XJTAG Chain Checker identifies
    – Connection Errors
    – Termination issues
    – Compliance pin problems

• Reviewing the design’s testability
  – XJTAG Access Viewer shows accessibility from JTAG
    – Shown on schematic in OrCAD Capture
Which steps are needed in DFT Assistant

• Select the BSDL Files
  – BSDL Files are Text Files that come from the Chip Vendor

• Define the TAP connections

• Categories the components
  – Mainly automatic with a few mouse clicks
Reporting in XJTAG DFT Assistant

Result of the JTAG-Chain check
XJTAG Access Viewer

Colored Nets show the test coverage
Where to find DFT Assistent

• OrCAD Capture
• Allegro CIS
• Mentor Pads
• Mentor Expedition
• Zuken CR8000
• Altium

https://www.xjtag.com/products/software/eda/

Or: Google helps… (mostly)
• DFT Assistant inside Capture
• XJAnalyser
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FlowCAD Deutschland
Mozartstr. 2
85622 Feldkirchen bei München
T +49 89 4563-7770
F +49 89 4563-7790
info@FlowCAD.de

FlowCAD Schweiz
Hintermättlistr. 1
5506 Mägenwil
T +41 56 485 91 91
F +41 56 485 91 95
info@FlowCAD.ch

FlowCAD Polen
ulica Sasiedzka 2A
80-298 Gdansk
T +48 58 732 74 77
F +48 58 732 72 37
info@FlowCAD.pl
Thank you!