UltraScale+ MPSoC as application accelerator

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Agenda

- Enclustra
- The Mandelbrot set
  - A short recap
- System
  - Ultrascale+ MPSoC
- Implementation
  - Multiplication in the FPGA
  - Data communication
Focused on FPGA Technology – Everything FPGA!

Founded in 2004 – successfully in business for 14 years!

Headquarters in Zürich, Switzerland

Branch offices in Germany, USA and China

2 Business units: FPGA Design Center, FPGA Solution Center

30 employees: 15 FPGA engineers plus 11 staff in Zurich, 4 employees abroad

Vendor-Independent
Enclustra Company Profile

- FPGA Design Center
  - Hardware (High-Speed, Analog, RF)
  - HDL firmware (VHDL, Verilog)
  - Embedded software (for FPGA processors)
- FPGA Solution Center
  - IP-Cores
  - FPGA & SoC Modules

FPGA? Enclustra!
The Mandelbrot set
The Mandelbrot set – short recap

- **Recursive sequence**
  \[
  z_0 = 0 \\
  z_{n+1} = z_n^2 + c
  \]

- **Iterative procedure to calculate the result**
  - **Stop after:**
    - The stop condition is reached
    - The number of iterations exceeded the specified limit

- **Split into real and imaginary part**
  \[
  u_{n+1} = u_n^2 - v_n^2 + c_u \\
  v_{n+1} = 2u_n v_n + c_v
  \]

- **Stop condition**
  \[
  u_n^2 + v_n^2 > 4
  \]
The calculation

- **The same calculation must be performed for each pixel**

- **From the number of iterations the color is chosen**

- **3 multiplications per iteration are necessary**
  - $2 \cdot u \cdot v$
  - $u^2 = u \cdot u$
  - $v^2 = v \cdot v$

- **Full HD picture**
  - $1920 \times 1080$ pixel = $2,073,600$ pixels
  - More then 6 million multiplications for 1 iteration
The system

- Enclustra Mercury+ XU1 Module
- Xilinx Zynq UltraScale+ MPSoC:
  - XCZU9EG-2FFVC900I
  - 2520 DSP Slices
  - 600’000 Logic Elements
- Large bit width needed for deep zooming-in
- Large number of iterations to show more details

100 iterations

4000 iterations
Key figures

- 64 bit fixpoint format
- Number range: -4.0 to +4.0
- 1 signed bit
- 2 bit integer value
- 61 bit fraction
- Maximum 4096 iterations
- Worst Case Full HD image: 25 billion multiplications
- Three 64x64 bit multipliers needed
  - UltraScale+ has only 48 bit wide multipliers (DSP48E2 slices)
These signals are dedicated routing paths internal to the DSP48E2 column. They are not accessible via general-purpose routing resources.
How to multiply 5 bit and 6 bit with a 3x3 bit multiplier

26*55=1430 (0b0101 1001 0110)

\[(a_1 + a_2) \times (b_1 + b_2) = a_1 b_1 + a_1 b_2 + a_2 b_1 + a_2 b_2\]
26*55=1430 (0b0101 1001 0110)

A = 26 (0b11010)

B = 55 (0b110111)

A) 26 = 24 + 2
B) 55 = 48 + 7
Multiplication Pipeline Example (3)

1) 2*7 = 14  \(0b001110\)
2) 2*6 = 12  \(0b001100\) (shift 3Bit)
3) 3*7 = 21  \(0b010101\) (shift 3Bit)
4) 3*6 = 18  \(0b010010\) (shift 6Bit)

26*55 = 1430 \(0b010110010110\)
- Requires 8 multiplications with 27x18 bit
- With addition total 10 clock cycles
- Great increase in efficiency through pipelining
Mercury+ XU1 Module – Zynq Ultrascale+ 9EG

4xARM A53

Mali GPU

FPGA Fabric

Baseboard

Display

DisplayPort
- Processing System
  - 4x ARM A53 @ 1333 MHz
  - Operating system: Ubuntu
  - GUI

- FPGA Fabric
  - Mandelbrot calculation
  - Clock frequency Cores 350MHz
  - Each core calculates one image line
  - Up to 80 cores
Software configures Mandelbrot controller
- Image size
- Max iterations
- Color chart

Mandelbrot controller controls Mandelbrot Cores
- Generates interrupt when image is finished

Up to 80 cores
- Each core calculates one image line
- Core converts number of iterations to an RGB value with color table
- Writes the finished pixels into framebuffer SDRAM via DMA
Challenges

- **Simulation of the design**
- **The calculation time per line varies greatly**
  - Worst case 4096 times longer
  - Sequence of completed lines is out of order
- **When the picture calculation has almost finished**
  - Only 1 core still working, all others are idle
  - Start with new frame before old one is completely finished
- **The pixels must be transferred from the FPGA to the display.**
- Data communication -

- Color format: RGB565
  - 16 bit per pixel
  - 4 MByte per picture
- Over 100 Mbyte/sec generated data
- DMA allows direct transfer of pixel data from FPGA to SDRAM
- Copying data manually
  - Only suitable for small amount of data

- Mandelbrot uses DMA to write directly to the framebuffer
  - No unnecessary copying of images
  - Special kernel driver provides direct access to the Linux framebuffer

- Image is transmitted by the operating system to the monitor via display port
Advantages of application acceleration

- Modern MPSoCs offer great flexibility
- They are excellently suited for demanding calculations
- The same design can be integrated into a smaller or larger FPGA, as the number of cores is variable
The UltraScale+ MPSoC

- Calculates 84 billion 64x64Bit multiplications per second
- Generates an average of 1 Gbit color data per second
- Power consumption ~35 Watt

Visit our booth to experience the demo live!
Everything FPGA.